Implementation of an Integrated FPGA Based Automatic Test Equipment and Test Generation for Digital Circuits

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Abstract- This paper describes the implementation of easy to use and reconfigurable automatic test equipment based on FPGA using Xilinx family. With respect to most of other ATEs, no microprocessor or microcontroller is fitted on the programmable resource. The testers are predominantly used to test digital PCBs or processors or Circuits, physically. The results are necessary to validate any Digital Hardware. The digital pattern generators & imported logic analyzers are very expensive for everybody involved in Electronics Design to afford, as they run into Lackhs of Rupees (more expensive than the Design cost itself). So, we need to evolve some low cost, Indigenous & accurate PC based equipment, which can perform the test vector generation, & provide required signals to test. We will be using Xilinx (Version 12.4) and FPGA for implementation of digital test pattern generation, since we can implement digital glue logic up to 200K gates & the design can be scaled up to 32 channels, without difficulty. This test system can easily be modified for use with any logic family, since the test hardware is essentially independent of the particular test chip. Thus the system is completely flexible for use in most small & medium-scale testing application. The test set for each IC is an exhaustive set of all possible input combinations; this ATE is used for SSI & MSI functions. Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

Keywords: ATE, digital pattern generator, switch matrix.

I. INTRODUCTION

The VLSI circuit manufacturer cannot guarantee the defect free integrated circuits(IC’s).This makes us to evolve a fast accurate means of testing such circuits. In a small-scale environment, it may not be feasible to invest large sums of money into complex IC testers. In labs till now we are having Digital testers which will test IC’s based on some non functional parameters like temperature, any short circuits in the IC etc. & are used for testing only Combinational circuits. In this paper, the validation is based on the functionality of IC. The digital pattern generator and logic analyzer are used to test the combinational, sequential circuits. This paper describes a versatile but inexpensive, testing system for standard digital IC’s 7400-series transistor-transistor logic (TTL) based on the the use the use of a FPGA. This tester can be economically implemented for small or medium-scale users of such IC’s & provides a quick but thorough checkout of most small & medium-scale functions with minimal operator action. Dedicated special-purpose hardware is minimal, allowing this tester to be implemented on virtually FPGA. Each IC is tested by applying test patterns to input pins of the chip & the resulting chip outputs are then examined for errors resulting from the stuck-at conditions or other functional errors. For Dedicated ATE, all input & output patterns are compacted & stored in a data base & are compared with the expected outputs, For Generalized ATE, the DUT output can be stored in the Logic analyzer & user need to check the functionality based on the input & output results. This ATE can be used to test the combinational and sequential circuits. The test set for each IC is an exhaustive set of all possible input combinations; this ATE is used for SSI & MSI functions. VLSI is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip.
stored in the memory. Along with appropriate clock signals if needed. Reconfigurable logic device has programmable interconnects so that user can realize desired function in it. It is also called programmable logic device (PLD) or field programmable gate array (FPGA). Recently logic capacity of PLD becomes large enough to realize various data processing functions within it. Although PLD’s performance is not as high as ASIC when it is designed for the same application, its re-programmability has advantages & many applications are proposed [2]. PLD system can be over 100 times faster than processor based system for applications with high parallelism [3,4]. This paper describes the design of ATE on FPGA, which produces the test patterns by using digital pattern generator (DPG), rather than storing the test patterns as a lookup table for specific IC.

III. DESIGN METHODOLOGIES

The proposed ATE system architecture mainly consists of frequency synthesizer, switch matrix, logic analyzer and control block for basic gates, combinational and sequential circuits. All the above modules are integrated into single unit as shown in figure 1 and implemented it on FPGA.

3.1 Digital Pattern Generator

The digital pattern generator is useful for functional testing, debug of new designs and failure analysis of existing designs. The digital pattern generator can be used early in the design cycle to substitute for system components that are not yet available. For example, a digital pattern generator might be programmed to send interrupts and data to a newly developed bus circuit when the processor that would normally provide the signals doesn’t yet exist. Digital Pattern Generator (DPG) consists of

- Frequency synthesizer
- Switch matrix
- Control blocks

3.1 Frequency synthesizer

Frequency synthesizer will produce different frequency signals by the excitation of a 4MHz clock signal. The clock signal has been generated from a crystal oscillator which generates six different frequencies ranging from 1 Hz to 1 MHz. Frequency Synthesizer is nothing but designing different counters so that required clock frequency can be obtained. Spartan2 FPGA consists of 4 MHz crystal oscillator. As shown in the figure 2, six different frequencies are generated first by using mod 4 counter 1 MHz clock. Use 1Mhz as a clock and give it to mod 10 counter to generate 100Khz in the same way three more mod 10 counters are used to obtain 10Khz, 1Khz and 100hz. Finally to generate 1hz mod 100 counter is used by giving 100hz as a clock.

![Block diagram of automatic test equipment](image1)

**Fig1. Block diagram of automatic test equipment for digital integrated circuits**

![Generation of different frequency signals](image2)

**Fig2. Generation of different frequency signals**

3.2 Switch Matrix

A switch matrix is used in test systems, in both design verification and manufacturing test, to route high frequency signals between the device under test (DUT) and measurement equipment. Since the signal routing and signal conditioning needs for a test system differ from design to design, Switch Matrices typically have to be custom designed by the test system engineer for each new test system. The variable frequencies from FSB output along with logic 1 and logic 0 are feed to switch matrix as shown in figure 3. The command from the control logic block to switch matrix is based on the DUT. Logic 1’s and logic 0’s are selected for the combinational circuits and different frequency signals are selected for sequential circuits. So the test hardware is essentially independent of the test chip. Changing from one logic family to another can be made by simply changing the command from the command register.
The command register will receive the input signals generated by the generalized sequential control block if from FPGA switches and enables the control block basic gates control block. Generalized combinational lines will be generated by the basic gates control block. The internal switch configuration of the switch matrix accordingly. Each control block generates the test patterns which are used as select input signals to all the eight multiplexers, three bits to each multiplexer. The control blocks will generate twenty-four bits from control block based on DUT. If the DUT is any basic gate then select lines will be generated by basic gates control block. If the DUT is combinational integrated circuit then select lines will be generated by generalized combinational control block. The select lines will be generated by generalized sequential control block if the DUT is sequential integrated circuit.

**3.4 Logic Analyzer**

A logic analyzer is an electronic instrument which displays signals of a digital circuit and used to check and analyze the test outputs. A logic analyzer may convert the captured data into timing diagrams, protocol decodes, state machine traces, assembly language, or correlate assembly with source-level software. One of the logic analyzer is a PC-based logic analyzer. The hardware connects to a computer through a USB or Ethernet connection and then relays the captured signals to the software on the computer as shown in figure 5. These devices are typically much smaller and less expensive, because they do not need dedicated displays or hardware input such as keyboards or knobs. Debuggers and hyper terminals offer additional functionalities along with displaying the output in bit format. Many digital designs, including those of ICs, are simulated to detect defects before the unit is constructed. The simulation usually provides logic analysis displays. Often, complex discreet logic is verified by simulating Inputs Andout Puts using boundary scan.

**IV. RESULTS**

The FSB, switch matrix, control logic & UART units of DPG are simulated & synthesized on Xilinx. This ATE is independent to test any logic family. The test system described in this paper was implemented & tested the logic circuits. The exhaustive testing method, although requiring more time & memory space than the other testing techniques, was selected for SSI functions to allow all single & multiple faults to be detected in any gate. In addition, this method accepts the ICs with scalable input pins. The testing time for each IC was found to be negligible, considering the time required for manual insertion & removal of the chip from the test socket.

**4.1 Case study of Basic gates IC**

The basic gates IC is tested by using above ATE design methodology & XOR gate waveform is shown in Figure 6. The results are as expected for XOR gate, hence we conclude that the device under test is verified for its functionality.

**Fig 3. Switch Matrix Block**

The internal switch configuration of switch matrix as explained in figure 4, consists of eight 8:1 multiplexers. Each multiplexer has six inputs from frequency synthesis block and other two are Vcc and ground. The select line signals for each multiplexer is generated from control block based on DUT. If the DUT is any basic gate then select lines will be generated by basic gates control block. If the DUT is combinational integrated circuit then select lines will be generated by generalized combinational control block. The select lines will be generated by generalized sequential control block if the DUT is sequential integrated circuit.

**Fig 4. Internal switch configuration of switch matrix**

This module consists of three control blocks namely basic gates control block, generalized combinational control block, generalized sequential control block. The control blocks will generate twenty-four bits from FPGA switches and enables the control block accordingly. Each control block generates different select line signals based on DUT.

**Fig 5. XOR gate waveform**
4.2 Case study of Multiplier IC

The multiplier IC is tested by using above ATE design methodology & multiplier IC waveform is shown in Figure 6. The results are as expected for multiplier IC, hence we conclude that the device under test is verified for its functionality.

![Multiplier waveform](image)

4.3 Case study of Sequential IC

The Sequential IC is tested by using above ATE design methodology & Sequential IC waveform is shown in Figure 7. The results are as expected for Sequential IC, hence we conclude that the device under test is verified for its functionality.

![Sequential waveform](image)

V. CONCLUSION

The reconfigurable and easy to use automatic test equipment is implemented using the FSB, switch matrix, control block & a host PC (Logic Analyzer). The test system can easily be modified for use with any logic family, since the test hardware is essentially independent of the particular test chip. Changing from one logic family to another can be made by changing the command on the control register. Thus the system is completely flexible for use in most small & medium-scale testing applications.

VI. REFERENCES


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